1. (amended) A method of forming a contact opening in a semiconductor device comprising at least a first gate and a second gate over a substrate, wherein the said first and second gates have sidewall spacers, the method comprising the steps of:

forming a dielectric liner layer over the semiconductor device;

forming a dielectric layer over the dielectric liner layer; and

patterning the dielectric layer and the dielectric liner layer without planarizing the dielectric layer to form a self-aligned contact window that exposes a surface of the substrate between the said first and second gates, wherein a dimension of the contact window at a top is greater than a distance between the sidewall spacers of the first gate and the second gate.

6. (amended) A method of forming a contact plug in a semiconductor device comprising at least a first gate and a second gate over a substrate, wherein the said first and second gates have sidewall spacers, the method comprising the steps of:

forming a dielectric liner layer conformal to a surface profile of the substrate and the said first and second gates;

forming a dielectric liner layer over the dielectric liner layer;

patterning the dielectric layer and the dielectric liner layer without planaring the dielectric layer to form a self-aligned contact window that exposes a surface of the substrate between said first and second gates, wherein a dimension of the contact window formed in the dielectric layer is greater than a distance between the sidewall spacers of the first gate and the second gate;

forming a polysilicon layer over the dielectric layer and filling the self-aligned contact window;

removing a portion of the polysilicon layer lying above the dielectric layer; and

removing a portion of the dielectric layer so that the contact plug is formed inside the self-aligned contact window.

12. (amended). A method of forming a contact plug in a semiconductor device comprising at least a first gate and a second gate over a substrate, wherein the said first and second gates have sidewall spacers, the method comprising the steps of:

forming a silicon nitride dielectric liner layer conformal to a surface profile of the substrate and the said first and second gates;

forming a silicon oxide dielectric layer over the substrate;

patterning the silicon oxide layer and the silicon nitride layer without planarizing the silicon oxide dielectric liner layer to form a self aligned contact wind that exposes a surface of the substrate between the said first and second gates, wherein a dimension of the contact window formed in the silicon oxide dielectric layer and the silicon nitride dielectric liner layer is greater than a distance between the sidewall spacers of the first gate and the second gate;

forming a polysilicon layer over the dielectric layer and filling the self-aligned contact window;

performing chemical-mechanical polishing to remove a portion of the polysilicon layer lying above the silicon oxide layer and a portion of the silicon oxide layer so that the landed plug is formed inside the self-aligned contact window.

15. (amended) A method of forming a contact opening in a semiconductor device comprising at least a first gate and a second gate, with sidewall spacers, over a substrate, and a thin liner oxide layer disposed conformal to the surface profile of the substrate and the said first and second gates, the method comprising the steps of:

forming a dielectric layer over the semiconductor device; and

patterning the dielectric layer without planarizing the dielectric layer to form a self-aligned contact window between the said first and second gates, wherein a dimension of the contact window at a top is greater than a distance between the sidewall spacers of the first gate and the second gate.

Present Status of the Application

Claims 1-19 remain pending of which claims 1, 6, 12 and 15 have been amended to more explicitly and more clearly describe the claimed invention. It is believed that no new matter is added by way of these amendments made to the claims or specification or otherwise to the application.

The Applicants have most respectfully considered the remarks set forth in this Office Action. Regarding the obviousness rejection, it is however strongly believed that the cited references are deficient to adequately teach the claimed features as recited in the amended claims. The reasons that motivate the above position of the Applicants are discussed in detail hereafter, upon which reconsideration of the claims is most earnestly solicited.

Discussion of Office Action Rejections

Claims 1-19 stand rejected under 35 U.S.C. § 103(a) as purportedly being unpatentable over Yoon et al. (US6,117,766, Yoon hereinafter) in view of Jeong (US 5,960,310). Applicant respectfully asserts that Yoon in view of Jeong is legally deficient for the purpose of rendering

claims 1, 6, 12 and 15 unpatentable for at least the reason that not every element of the claims was taught or suggested by cited references such that the invention as a whole would have been obvious to one of ordinary skill in the art. More specifically, the present invention teaches in claims 1, 6, 12 and 15 substantially "...forming a dielectric liner layer over the semiconductor device; ....patterning the dielectric layer and the dielectric liner layer without planarizing the dielectric layer to form a self-aligned contact window that exposes a surface of the substrate between the said first and second gates, wherein a dimension of the contact window at a top is greater than a distance between the sidewall spacers of the first gate and the second gate...".

Contrary to the Office's assertion, the contact window of Yoon is not a self-aligned contact window since the contact hole of Yoon is narrower than the distance between the sidewall spacers of the two neighboring gate structures. The present invention, on the other hand, teaches a formation of a self-aligned contact window, wherein a dimension of the contact window at a top is greater than a distance between the sidewall spacers of the first gate and the second gate. To accomplish the formation of a self-aligned contact window with the contact window at the top larger than the distance between the two gates, the present invention teaches forming a liner layer over the semiconductor device, followed by forming a dielectric layer over the liner layer. Without planarizing the dielectric layer, portions of the liner layer and the dielectric layer are etched to form the self-aligned contact window. Further, the dielectric liner layer is etched to form a plurality of spacers 204a and passivation layers 204b for the gate electrodes (pg. 8, line 6-14). The self-aligned contact window of the present invention is thereby formed utilizing a high etching selectivity between the dielectric liner layer and the dielectric layer, and the gate electrodes are much better protected with the dielectric liner layer. As recognized by the Office,

Yoon fails to disclose a dielectric liner for at least the reason that Yoon is not teaching a method of forming a contact hole such that a dimension of the contact window at a top is greater than a distance between the sidewall spacers of the first gate and the second gate.

Seeking to remedy the deficiency in Yoon, the Office then relies on the teaching of Jeong. However, similar to Yoon, Jeong also fails to teach a dimension of the contact window at a top is greater than a distance between the sidewall spacers of the first gate and the second gate. As a matter of fact, the contact hole 82 of Jeong is formed over the patterned wiring layers 75a, 95a, 115a (Fig. 4D, col. 7, line 1-3), whereas the contact hole of the present invention is a self-aligned contact formed between two neighboring gate electrodes. Therefore, even Jeong teaches a first insulating layer 77 that is conformal to the surface of the substrate, the insulating layer 77 is not etched to form a plurality of spacers and passivation layers for better protection for the gate electrodes as taught in the present invention. Moreover, Jeong also teaches after filling the recess in the first insulating layer 77, an etch back is conducted to planarize the first insulating layer 77, followed by forming a third insulating layer 82 and then forming the contact holes 82. The present invention, however, teaches patterning the dielectric layer without planarizing the dielectric layer to form a self-aligned contact window. Jeong thereby teaches away from the present invention. Thus, persons skilled in the art will not be motivated to combine Yoon with Jeong.

In view of the foregoing, Applicant contends that the prior art cited by the Office, neither alone nor in combination teaches or suggests every element of claims 1, 6, 12 and 15. Applicants therefore respectfully request the withdrawal of the rejection under 35 U.S.C. § 103(a) of claims 1, 6, 12 and 15 and claims 2-5, 7-11, 13-14 and 16-19 depending therefrom.

CONCLUSION

For at least the foregoing reasons, it is believed that the presently pending claims 1-19 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned. Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

Respectfully submitted,

Date : March 4, 2003

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please amend claims 1, 6, 12 and 15 as follow:

1. (amended) A method of forming a contact opening in a semiconductor device comprising at least a first gate and a second gate over a substrate, wherein the said first and second gates have sidewall spacers, the method comprising the steps of:

forming a dielectric liner layer over the semiconductor device;

forming a dielectric layer over the dielectric liner layer; and

patterning the dielectric layer and the dielectric liner layer without planarizing the dielectric layer[,] to form a self-aligned contact window that exposes a surface of the substrate between the said first and second gates, wherein a dimension of the contact window at a top is greater than a distance between the sidewall spacers of the first gate and the second gate.

6. (amended) A method of forming a contact plug in a semiconductor device comprising at least a first gate and a second gate over a substrate, wherein the said first and second gates have sidewall spacers, the method comprising the steps of:

forming a dielectric liner layer conformal to a surface profile of the substrate and the said first and second gates;

forming a dielectric liner layer over the dielectric liner layer;

patterning the dielectric layer and the dielectric liner layer without planaring the dielectric layer[,] to form a self-aligned contact window that exposes a surface of the substrate between said first and second gates, wherein a dimension of the contact window formed in the dielectric layer is greater than a distance between the sidewall spacers of the first gate and the second gate;

forming a polysilicon layer over the dielectric layer and filling the self-aligned contact window;

removing a portion of the polysilicon layer lying above the dielectric layer; and

removing a portion of the dielectric layer so that the contact plug is formed inside the self-aligned contact window.

12. (amended) A method of forming a contact plug in a semiconductor device comprising at least a first gate and a second gate over a substrate, wherein the said first and second gates have sidewall spacers, the method comprising the steps of:

forming a silicon nitride dielectric liner layer conformal to a surface profile of the substrate and the said first and second gates;

forming a silicon oxide dielectric layer over the substrate;

patterning the silicon oxide layer and the silicon nitride layer without planarizing the silicon oxide dielectric liner layer[,] to form a self aligned contact wind that exposes a surface of the substrate between the said first and second gates, wherein a dimension of the contact window formed in the silicon oxide dielectric layer and the silicon nitride dielectric liner layer is greater than a distance between the sidewall spacers of the first gate and the second gate;

forming a polysilicon layer over the dielectric layer and filling the self-aligned contact window;

performing chemical-mechanical polishing to remove a portion of the polysilicon layer lying above the silicon oxide layer and a portion of the silicon oxide layer so that the landed plug is formed inside the self-aligned contact window.

15. (amended) A method of forming a contact opening in a semiconductor device comprising at least a first gate and a second gate, with sidewall spacers, over a substrate, and a thin liner oxide layer disposed conformal to the surface profile of the substrate and the said first and second gates, the method comprising the steps of:

forming a dielectric layer over the semiconductor device; and

patterning the dielectric layer without planarizing the dielectric layer[,] to form a self-aligned contact window between the said first and second gates, wherein a dimension of the contact window at a top is greater than a distance between the sidewall spacers of the first gate and the second gate.